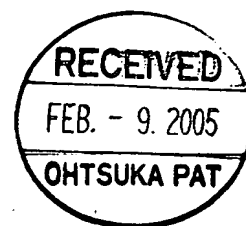


PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY



PCT

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43bis.1)

To:

OHTSUKA Yasunori

**7th FL., SHUWA KIOICHO PARK
BLDG., 3-6, KIOICHO, CHIYODA-
KU, Tokyo
1020094
Japan**

Date of mailing
(day/month/year)

08.02.2005

Applicant's or agent's file reference

P204-0467WO

FOR FURTHER ACTION

See paragraph 2 below

International application No.

PCT/JP2004/018982

International filing date (day/month/year)

14.12.2004

Priority date (day/month/year)

26.12.2003

International Patent Classification (IPC) or both national classification and IPC

Int.Cl.⁷ **H01L21/20, H01L27/12, H01L29/161, H01L29/786**

Applicant

CANON KABUSHIKI KAISHA

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- ☒ Box No. VI Certain documents cited
- ☐ Box No. VII Certain defects in the international application
- ☐ Box No. VIII Certain observations on the international application

2. FURTHER ACTION

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1bis(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

3. For further details, see notes to Form PCT/ISA/220.

Date of completion of this opinion

24.01.2005

Name and mailing address of the ISA/JP

Japan Patent Office

Authorized officer

SHINGO FUCHI

4L

2933

3-4-3, Kasumigaseki, Chiyoda-ku, Tokyo 100-8915, Japan

Telephone No. +81-3-3581-1101 Ext. 3496

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

International application No.

PCT/JP2004/018982

Box No. I Basis of the opinion

1. With regard to the **language**, this opinion has been established on the basis of the international application in the language in which it was filed, unless otherwise indicated under this item.

- ☐ This opinion has been established on the basis of a translation from the original language into the following language _____, which is the language of a translation furnished for the purposes of international search (under Rules 12.3 and 23.1(b)).

2. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application and necessary to the claimed invention, this opinion has been established on the basis of:

a. type of material

- ☐ a sequence listing
☐ table(s) related to the sequence listing

b. format of material

- ☐ in written format
☐ in computer readable form

c. time of filing/furnishing

- ☐ contained in the international application as filed.
☐ filed together with the international application in computer readable form.
☐ furnished subsequently to this Authority for the purposes of search.

3. ☐ In addition, in the case that more than one version or copy of a sequence listing and/or table relating thereto has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

4. Additional comments:

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

International application No.

PCT/JP2004/ 018982

Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims	<u>1 - 38</u>	YES
	Claims		NO
Inventive step (IS)	Claims	<u>7, 18, 27, 37</u>	YES
	Claims	<u>1 - 6, 8 - 17, 19 - 26, 28 - 36, 38</u>	NO
Industrial applicability (IA)	Claims	<u>1 - 38</u>	YES
	Claims		NO

2. Citations and explanations

D1:JP 2003-178977 A(MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.)

2003.06.27, [0015]-[0044], Figs. 2-4

D2:JP 2003-282464 A(SEIKO EPSON CORPORATION)

2003.10.03, [0010]-[0033], Figs. 1-4

D3:EP 1248294 A2(CANON KABUSHIKI KAISHA)

2002.10.09, [0042]-[0062], Figs. 1A-1E

D4:JP 2003-282463 A(SEIKO EPSON CORPORATION)

2003.10.03, [0010]-[0028], Figs. 1-2

Claims 1-4, 8-13, 19

The subject matter of claims 1-4, 8-13, 19 does not appear to involve an inventive step in view of the D 1 and the D2 cited in the ISR.

D1 discloses the semiconductor layer structure comprising; the porous Si buffer layer on the Si substrate, the SiGe strain induction layer on the porous Si buffer layer, and the strained Si layer on the SiGe strain induction layer.

D2 discloses that the porous SiGe buffer is used as a buffer layer.

The technical feature in D1 and D2 are concerned with mutually related technical fields in a lattice-mismatched semiconductor hetero-epitaxial layer structures using Si and Ge. Therefore, the skilled person in the art would easily conceive the idea of employing the porous SiGe buffer in D2 to substitute the SiGe strain induction layer disclosed in D1.

And if the skilled person in the art would conceive the idea of employing the porous SiGe buffer in D2 to substitute the SiGe strain induction layer disclosed in D1, it is obvious that the step of porosifying the SiGe is carried out before the growth of strained Si layer.

Claim 5

The subject matter of claim 5 does not appear to involve an inventive step in view of the D1 and the D2 cited in the ISR.

D1 and D2 disclose that the porous semiconductor layer is formed by anodizing the semiconductor layer.

Claim 6

The subject matter of claim 6 does not appear to involve an inventive step in view of the D1 and the D2 cited in the ISR.

D2 discloses that the one of strain relaxation method is annealing.

WRITTEN OPINION OF THE
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International application No.

PCT/JP2004/018982

Box No. VI Certain documents cited

1. Certain published documents (Rules 43bis.1 and 70.10)

<u>Application No. Patent No.</u>	<u>Publication date (day/month/year)</u>	<u>Filing date (day/month/year)</u>	<u>Priority date (valid claim) (day/month/year)</u>
JP 2004-342975 A E, X	02.12.2004	19.05.2003	

2. Non-written disclosures (Rules 43bis.1 and 70.9)

<u>Kind of non-written disclosure</u>	<u>Date of non-written disclosure (day/month/year)</u>	<u>Date of written disclosure referring to non-written disclosure (day/month/year)</u>
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Supplemental Box

In case the space in any of the preceding boxes is not sufficient.
Continuation of: V. 2

Claim 7

The subject matter of claim 7 is neither disclosed in any of the documents cited in the ISR nor obvious to a person skilled in the art. In particular, the method comprising; the step of stacking another strain induction layer on the porous strain induction layer is not disclosed in D1 and D2.

Claims 14-17

The subject matter of claims 14-17 does not appear to involve an inventive step in view of the D1-D3 cited in the ISR.

D3 discloses the method of transferring the strained Si layer from first member to a second member by separating the porous semiconductor layer.

The technical feature in D1 and D3 are concerned with mutually related technical fields in a method of fabrication of strained Si layer. Therefore, the skilled person in the art would easily conceive the idea of employing the technical feature of transferring the strained Si layer in D3 to add the invention disclosed in D1.

Claim 18

The subject matter of claim 18 is neither disclosed in any of the documents cited in the ISR nor obvious to a person skilled in the art. In particular, separating at a defect generation portion in an interface between a strain induction porous layer and porous semiconductor layer is not disclosed in D3.

Claims 20-26, 28-32, 38

The subject matter of claims 20-26, 28-32, 38 does not appear to involve an inventive step in view of the D1, D2 and D4 cited in the ISR.

D4 discloses the multi porous buffer layer between substrate and epitaxial layer.

The technical feature in D1, D2 and D4 are concerned with mutually related technical fields in a lattice-mismatched semiconductor hetero-epitaxial layer structures using Si and Ge. Therefore, the skilled person in the art would easily conceive the idea of employing the multi porous buffer in D4 to substitute the SiGe strain induction layer disclosed in D1 or D2. And the number or material of buffer layer is the matter of design variation.

Claim 27

The subject matter of claim 27 is neither disclosed in any of the documents cited in the ISR nor obvious to a person skilled in the art. In particular, the method comprising; the step of stacking another strain induction layer on the porous strain induction layer is not disclosed in D1, D2 and D4.

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.
Continuation of: V. 2

Claim 33-36

The subject matter of claims 33-36 does not appear to involve an inventive step in view of the D1-D4 cited in the ISR.

D3 discloses the method of transferring the strained Si layer from first member to a second member by separating the porous semiconductor layer.

The technical feature in D1 and D3 are concerned with mutually related technical fields in a method of fabrication of strained Si layer. Therefore, the skilled person in the art would easily conceive the idea of employing the technical feature of transferring the strained Si layer in D3 to add the invention disclosed in D1.

Claim 37

The subject matter of claim 37 is neither disclosed in any of the documents cited in the ISR nor obvious to a person skilled in the art. In particular, separating at a defect generation portion in an interface between a strain induction porous layer and porous semiconductor layer is not disclosed in D3.